# REMARKS

## 1.Present Status of the Application

Claims 1-21, 25-30, 33-52 and 56-60 are rejected under 35 U.S.C. 102(a) as being anticipated by Akagawa. (US Patent No. 6,121,688) Claims 1, 23, 30-32 and 54 are rejected under 35 U.S.C. 102(a) as being anticipated by Shanefield. (US Patent No. 4,866,501) Claims 24, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanefield as applied to claims 23 and 54. Upon this response, claims 1-17, 21, 23-40, 43-48, 52, 54-60, and 139-142 remain pending in the present application.

## 2.Response To Objections/Rejections

Applicants respectfully traverse the rejections for at least the reasons set forth below.

### Response To Claim Rejections Under 35 U.S.C. Section 102

#### I. Discussion for Claim 1

As recited above, independent claim 1 is recited below:

1. A chip package structure comprising:
a substrate having a surface;
***only a die***, wherein the die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas ***the backside of the die is adhered to the surface of the substrate,*** and ***the surface of the substrate has an area larger than that of the active surface of the die***; and
a thin-film circuit layer located over the substrate and the die and having an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a

plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die.

***(emphasis added)***

Applicants respectfully assert that the chip package claimed in the present invention patentably distinguishes over the citations by Akagawa and by Shanefield, because the citations fail to disclose these features emphasized above (in bold).

In the citations by Akagawa and by Shanefield, *a chip package has two dies mounted on a substrate.* (See FIG.6 in Akagawa's referince and FIGS. 1-3 in Shanefield's reference) It is acknowledged that the present invention discloses a different method and structure than the prior art since *after the singulation process is preformed, the completed chip structure has only one chip 120 mounted on the substrate 110.* (from paragraph [0036] and FIG. 1I) *The surface 112 of the substrate 110 has an area larger than that of the active surface 122 of the chip 120.* The disclosure by Akagawa or by Shanefield *fails to teach, suggest, or hint the above feature.* Therefore, Applicants respectfully traverse the rejection under 35 U.S.C. 102 (a).

Putting several dies on one substrate, taught by Akagawa and Shanefield, has a following drawback. If there are two chips bonded on a substrate, the performance of one chip may be affected by the extra heat generated by the other chip. However, the present invention discloses that there can be only one chip bonded on a substrate, and, therefore, the performance of the chip can not be affected by other heat sources and it is effective that the heat generated by the chip is dissipated. Such a design philosophy is not seen in the prior art.

**II. Discussion for Claim 30**

As recited above, independent claim 30 is recited below:

30. A chip package structure comprising:

a substrate having a surface;

a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of each die is adhered to the surface of the substrate;

a thin-film circuit layer located over the substrate and the die and having an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die; and

***at least one passive device positioned inside or on the thin-film circuit layer,*** wherein ***the passive device is selected from a group consisting of an inductor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).***

***(emphasis added)***

Applicants respectfully assert that the chip package claimed in the present invention patentably distinguishes over the citations by Akagawa and by Shanefield, because the citations fail to disclose these features emphasized above (in bold).

In the citations, Akagawa only teaches *a decoupling capacitor and a resistor can be built in a thin-film circuit layer*. (from Column 8 and Lines 37-41) However, in the present invention, besides a capacitor and a resistor, *a passive device selected from a group consisting of an inductor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS) also can be built inside or on a thin-film circuit layer*. The disclosure by Akagawa or by Shanefield *fails to*

*teach, suggest, or hint the above feature*. Therefore, Applicants respectfully traverse the rejection under 35 U.S.C. 102 (a).

**Response To Claim Rejections Under 35 U.S.C. Section 103**

**I. Discussion for Claim 1**

Applicants respectfully assert that the chip structure claimed in the present invention patentably distinguishes over the disclosures by Akagawa and by Shanefield, because the disclosures fail to disclose these features emphasized in claim 1 (in bold).

One of the features in accordance with the present invention is that *after a singulation process is preformed, the completed chip structure has only one chip mounted on a substrate*. However, both of the citations by Akagawa and by Shanefield fail to teach, suggest or hint the above feature. Therefore, even though the citations by Akagawa and by Shanefield are combined, the subject matters claimed in the present invention can not be attained.

**II. Discussion for Claim 30**

Applicants respectfully assert that the chip structure claimed in the present invention patentably distinguishes over the disclosures by Akagawa and by Shanefield, because the disclosures fail to disclose these features emphasized in claim 30 (in bold).

One of the features in accordance with the present invention is that *a passive device selected from a group consisting of an inductor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS) is built inside or on a thin-film circuit layer*. However, both of the

citations by Akagawa and by Shanefield fail to teach, suggest or hint the above feature. Therefore, even though the citations by Akagawa and by Shanefield are combined, the subject matters claimed in the present invention can not be attained.

As a result, Applicants consider that the citations taught by Akagawa and Shanefield, alone or combination as a whole, do not render the claimed subject matters. For at least the foregoing reasons, Applicants respectfully submit independent claims 1 and 30 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-17, 21, 23-29, 31-40, 43-48, 52, 54-60, and 139-142 patently define over the prior art as well.

**Application No.: 10/055,568** **Docket No.: JCLA8533**

## CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-17, 21, 23-40, 43-48, 52, 54-60, and 139-142 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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